IN THE TITLE:

At page 1, line 1, please replace the Title in its entirety and replace with the following Title:

-- METHOD OF PREVENTING DIFFUSION OF COPPER THROUGH A TANTALUM-COMPRISING BARRIER LAYER --

IN THE SPECIFICATION:

Please replace the paragraph at page 7, lines 7 - 23, with the following rewritten paragraph:

-- U.S. Patent ~~Application, Serial No. 08/511,825~~ No. 5,962,923 of Xu et al.. ~~filed August 7, 1995~~, issued October 5, 1999, assigned to the Assignee of the present invention, and hereby incorporated by reference in its entirety, describes a method of forming a titanium nitride-comprising barrier layer which acts as a carrier layer. The carrier layer enables the filling of apertures such as vias, holes or trenches of high aspect ratio and the planarization of a conductive film deposited over the carrier layer at reduced temperatures compared to prior art methods. The Xu et al. preferred embodiment carrier layer is a Ti/TiN/Ti three layered structure which is deposited using ion deposition (or ion metal plasma) sputtering techniques. Figure 1 of the present application shows a schematic of a cross-sectional view of a contact via which includes the carrier layer of Xu et al. In particular, Figure 1 shows an exemplary contact 118 formed in a high aspect ratio aperture 113. Specifically, aperture 113 has an aspect ratio of about 5:1, where dimension 120 is about 0.25 μ wide and dimension 122 is about 1.2 μ. The contact 118 includes at least two sub-elements. A carrier layer 100, which also acts as a barrier layer, and a conductive material 119 which has been deposited over the carrier layer 100, to fill the volume of the aperture remaining after the carrier layer has been deposited. --

Please insert the following paragraph, taken from U.S. Patent No. 5,962,963 (the subject matter of which was incorporated by reference in its entirety into the present application), at page 8, after the end of line 6 and prior to the beginning of line:

-- To provide the three layer structure of carrier layer 100 as shown in Figure 1, all three layers 100 are preferably deposited in a single chamber in a continuous process. This may be accomplished, in the case of a titanium based carrier layer, by following the steps of sputtering a titanium target, ionizing at least a portion of the titanium (10 % to 100 %) before it is deposited on the substrate, attracting the ionized target material to the substrate and forming the first sublayer therewith; then introducing a sufficient quantity of a reactive gas, preferably nitrogen, into the chamber as sputtering and ionization continues and thereby causing all of the material sputtered from the target to react with the gas to form a compound film layer of TiN on the substrate; and then stopping the flow of reactive gas to the chamber while still sputtering the target and ionizing the sputtered target material to form a film layer on the substrate composed of both the base target material, preferably Ti and a reacted product, preferably TiN. Once the Ti/TiN sub-layer has been formed to a sufficient thickness, the power to the system is shut off to stop the sputtering process. --

Please replace the paragraph at page 9, lines 14 - 27, with the following rewritten paragraph:

-- The method is particularly applicable to the sculpturing of barrier layers, wetting layers and conductive layers upon semiconductor feature surfaces. When the conductive layer is tungsten and the barrier layer is titanium, using the method to deposit the titanium layer, so that the titanium is not contaminated by impurities sputtered off of surfaces adjacent the bottom of a contact via, for example, prevents an increase in the resistivity of the contact. When the conductive layer is aluminum and the underlying layer is a titanium wetting layer, use of the method to deposit the titanium avoids contamination of the titanium wetting layer by oxygen sputtered off of adjacent silicon dioxide surfaces during the titanium. An aluminum layer subsequently applied over the non-

contaminated titanium layer will flow better over the titanium layer. When the conductive layer is copper and the underlying layer is a tantalum barrier layer, for example, the method enables deposition of ~~an~~ a non-contaminated and conformal tantalum barrier layer, even at small feature size and high aspect ratio. --

Please replace the paragraph at page 11, line 20, through page 12, line 12, with the following rewritten paragraph:

-- A conductive material seed layer, and particularly a copper seed layer applied to the feature may be accomplished using the same sculpturing technique as that described above with reference to the barrier layer and wetting layer. Sculpturing of a copper seed layer is especially important when the copper fill is to be achieved by electroplating ~~:~~ , chemical vapor deposition (CVD), PVD (for example , the copper deposition technique described in applicants' ~~co-pending application Serial No. 08/855,059~~ U.S. Patent No. 6, 605,197, issued August 12, 2003) or a combination of these methods. It is necessary to have a continuous conformal seed layer. Without sculpturing of the copper seed layer, there is typically too much overhang of deposited material at the top of a contact via. This overhang leads to closure of the via opening prior to complete fill of the via, leaving voids inside the contact. If there is too much sputtering of the copper seed layer, this creates an absence of seed layer at the bottom of the via. Absence of copper seed layer causes voids to form at the bottom of the via ~~when~~ due to lack of copper growth in that area. (When the copper fill is deposited using electroplating, there is a lack of current for electroplating in areas where there is no copper seed layer.) The present method provides a continuous conformal seed layer. Substrate temperature is critical during the deposition and sculpturing of a copper seed layer, to avoid dewetting of the copper from the barrier layer surface. Preferably the substrate temperature during deposition and sculpturing of a copper seed layer is less than about 500 °C, and more preferably less than about 200°C. --

Please replace the paragraph beginning at page 12, lines 18 - 21, with the following rewritten paragraph.

-- Figure 2 illustrates, in schematic format, an apparatus of the kind which can be used to obtain ionization of sputtered target atoms prior to their deposition on a substrate and to attract the ionized material to the substrate. Figure 2 is a prior art drawing taken from U.S. Patent ~~Application, Serial No. 08/511,825~~ No. 5,962,923 of Xu et al. , issued October 5, 1999 . --

Please replace the paragraph at page 13, lines 14 - 21, with the following rewritten paragraph:

-- Tailoring of such thin layers using physical vapor deposition (PVD) techniques has been of particular interest in recent years due to the many desirable properties of materials applied using PVD. Ion deposition sputtering, also known as IMP, has been used to enable PVD application of material layers in features having small feature size ~~a~~ and high aspect ratios. However, ion deposition sputtering can have adverse side effects in terms of erosion via sputtering of underlying layers which are contacted by the ion deposition sputtered material. Further, the material eroded away from the underlying layer can contaminate adjacent surfaces of the feature. --

Please replace the paragraph at page 13, line 22, through page 14, line 13, with the following rewritten paragraph:

-- The present method for applying ~~a~~ an ion deposition sputtered sculptured layer of material on a semiconductor feature surface avoids sputtering of the substrate on which the ion deposition layer is deposited. The method is particularly useful in the deposition of barrier layers at the bottom of a via, where contamination from adjacent surfaces during deposition of the barrier layer can ultimately increase resistivity of the contact. The method is particularly useful in the deposition of a barrier layer when a conformal relatively uniform deposition is required to prevent diffusion of the material used as the conductive layer into adjacent dielectric materials. The method is particularly

useful in the deposition of a wetting layer when contamination of the wetting layer affects the ability of the layer to perform the wetting function. The method is particularly useful in the deposition of a conductive seed layer when contamination of the seed layer prevents the formation of a proper crystal structure in subsequently deposited conductive material. Further, in instances where the feature size is small and the aspect ratio is high and it is necessary to obtain a continual conformal seed layer of conductive material over the feature surface, the ability to sculpture the conformal layer is especially advantageous, as is the case when the conductive material is copper. --

Please replace the paragraph at page 15, lines 12 - 16, with the following rewritten paragraph:

-- The method of the present invention is not intended to be limited to applications in which copper is the conductive layer, however. The avoidance of the erosion of underlying layers during the deposition of barrier layers and metal conductive seed layers and fill layers is applicable to other systems such as an aluminum conductive layer used in combination with a Ti/TiN barrier layer, for example. --

Please replace the paragraph at page 18, lines 7 - 24, with the following rewritten paragraph:

-- To form the barrier layer structure of the present invention, the processing elements shown in Figure 2 can be operated within one of the low pressure process chambers contained within an Endura® Integrated Processing System. With reference to Figure 2, the low pressure process chamber for forming the barrier layer of the present invention employs a standard sputter magnet 210 (to confine the sputtering plasma, enabling an increased sputtering rate) and a tantalum sputtering target cathode 212 of about 14 inches (35.5 cm) in diameter, with a DC power 213 applied to this cathode over a range from about 0.5 kW to about 8 kW. The substrate, 218 was an 8 inch (200 mm) diameter silicon wafer, having a 1.2 μm thick layer of silicon dioxide dielectric overlying the silicon wafer. The dielectric layer had been patterned to contain contact vias which were 0.35 μm in

diameter at the bottom and 1.2 μm in height. The substrate wafer was placed a distance of about 5 inches (13 cm) from target cathode 212. A high density, inductively coupled RF plasma was generated in the region between the target cathode 212. A high density, inductively coupled RF plasma was generated in the region between the target cathode 212 and the substrate 218 by applying RF power ~~213~~ 216 over a range from about 100 kHz to about 60 MHz (preferably from about 2 MHz to about 13.56 MHz) to a single or multiple turn metal coil strip 214 at a wattage ranging from about 0.5 kW to about 6 kW (and preferably ranging from about 1.5 kW to about 4 kW). Preferably the ~~strip~~ coil strip 214 consists of less than 3 to 4 turns. --

Please replace the paragraph at page 18, line 25, through page 19, line 1, with the following rewritten paragraph:

-- A substrate bias voltage ranging from 0 to about -300 V DC may be applied to the substrate, typically by applying RF power 222 to the platen 220 on which the substrate 218 sits. When a bias voltage is applied, a ~~D.C.~~ DC substrate bias is created which attracts ions from the plasma to the substrate 218. --

Please delete the Abstract, at page 29, lines 6 - 28, with the following rewritten Abstract:

-- We disclose a method of applying a sculptured layer of material on a semiconductor feature surface using ion deposition sputtering, wherein a surface onto which the sculptured layer is applied is protected to resist erosion and contamination by impacting ions of a depositing layer. A first protective layer of material is deposited on a substrate surface using traditional sputtering or ion deposition sputtering, in combination with sufficiently low substrate bias that a surface onto which the layer is applied is not eroded away or contaminated during deposition of the protective layer. Subsequently, a sculptured second layer of material is applied using ion deposition sputtering at an increased substrate bias, to sculpture a shape from a portion of the first protective layer of

material and the second layer of depositing material. The method is particularly applicable to the sculpturing of barrier layers, wetting layers, and conductive layers upon semiconductor feature surfaces. --